REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated May 11, 2004. By the present Amendment, claim 1 has been amended to incorporate the subject matter of claim 3 (with claim 3 correspondingly being canceled to avoid redundancy). Claims 4 and 5 have also been amended to further clarify the invention. In addition, a new dependent claim 6, a new independent claim 7 and two additional new dependent claims 8 and 9 have been added to further define the invention.

Briefly, the pending claims of the present application are directed to the feature of a power-down mode shown, for example, in Fig. 11. As described in paragraphs 57 and 63 of the Specification, Fig. 11 shows the power-down mode (PDM) operation for the circuit VCL Limiter Control Circuit CTL1 shown in the upper right hand corner of Fig. 4. In particular, as shown by an arrow in Fig. 11 connecting the rise time for the clock enable CKE signal and the rise of the signal LC4 (which turns on the VCL Limiter circuit VCL4 shown in Fig. 4), the turn on of the VCL4 circuit is in synchronization with the rise time of the clock enable signal CKE prior to the rise time of the clock CLK at t10 which begins the end of the power-down mode PDMB). The reason for this is discussed in paragraph 63 as follows:

> "The signal CKE must be set to "1" earlier than the rise of the clock signal CLK by a set-up time (usually two to three ns). This means that the signal LC4 is raised earlier if the end of the power-down mode is judged based on the signal CKE than if the end of the mode is determined as per the signal PDMB. Since there is a possibility that a bank active command or a like command may be input during the clock cycle immediately after the power-down mode

end command, the voltage limiter circuit VCL4 should preferably be turned on earlier than usual in preparation for the command input."

Reconsideration and allowance of amended claim 1 and its dependent claims 2 and 6 over Fujioka (USP 5804893) is respectfully requested. By the present Amendment, claim 1 has been amended to incorporate the subject matter of claim 3 of "wherein said voltage limiter circuit starts operating in synchronism with a rising edge of said clock enable signal." This effectively defines the above-noted feature shown in Fig. 11 of the synchronizing the rise of the clock enable CKE signal with the turn on of the voltage limiter, rather than with the clock signal. New dependent claim 6 even further defines this by virtue of reciting:

"wherein said rising edge of said clock enable signal is prior to a rising edge of the external clock signal which terminates the power down mode."

The primary cited reference to Fujioka is completely devoid of any such features. Although Fujioka utilizes internal voltage reduction circuits such as identified with the numerals 10-1 to 10-n, he fails to teach or suggest the claimed features regarding the operation of the voltage limiter in accordance with the rise time of the CKE signal. Accordingly, reconsideration and removal of the rejection of claim 1 and its dependent claims 2 and 6 is respectfully requested.

Reconsideration and allowance of amended independent claim 4 is also respectfully requested. By the present Amendment, claim 4 has been amended to include the recitation of:

"wherein a voltage limiter in said first power supply circuit starts operating in synchronism with a clock enable signal applied to said

> synchronous DRAM prior to receipt of a power down mode end command by said synchronous DRAM."

Again, nothing in Fujioka teaches or suggest such an operation of the voltage limiter in synchronism with the clock enable signal. Therefore, again, reconsideration and allowance of independent claim 4 is respectfully requested.

Reconsideration and allowance of independent claim 5, as amended, is also respectfully requested. By the present Amendment, claim 5 has been amended to include the feature:

> "means for turning on a voltage limiter in one of said first or second power supply circuits prior to receipt of a power down mode end command being applied to the synchronous DRAM."

It is respectfully submitted that Fujioka completely lacks any teaching or suggestion of such a means for turning on a voltage limiter as defined by amended claim 5. Therefore, reconsideration and allowance of independent claim 5 is also respectfully requested.

Similarly, reconsideration of the new independent claim 7 and its dependent claims 8 and 9 is also respectfully requested. Like claim 5, claim 7 includes the limitation of:

> "means for turning on the voltage limiter circuit earlier than receipt of a power down mode end command being received by the control circuit."

As noted above, Fujioka completely lacks any suggestion of this claimed means. Similarly, Fujioka lacks any suggestion of the further detailed features defined by the dependent claims 8 and 9 concerning the start of the operation of the voltage limiter

in synchronism with the rising edge of the clock enable signal. Accordingly, reconsideration and allowance of these newly presented claims 7-9 is also respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 501.37021VV4), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Gregory E. Montone
Reg. No. 28,141

GEM/dlt

1300 North Seventeenth Street, Suite 1800
Arlington, Virginia 22209
Telephone: (703) 312-6600
Facsimile: (703) 312-6666